37647
25873

2048 BIT ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

1602A–ELECTRICALLY PROGRAMMABLE
1702A–ERASABLE & ELECTRICALLY REPROGRAMMABLE

- **Fast Programming -- 2 minutes for all 2048 bits**
- **All 2048 bits guaranteed * programmable -- 100% factory tested**
- **Fully Decoded, 256x8 organization**
- **Static MOS -- No Clocks Required**
- **Inputs and Outputs DTL and TTL compatible**
- **Three-state Output -- OR-tie Capability**
- **Simple Memory Expansion -- Chip select input lead**

The 1602A and 1702A are 256 word by 8-bit electrically programmable ROMs ideally suited for uses where fast turn-around and pattern experimentation are important. The 1602A and 1702A undergo complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

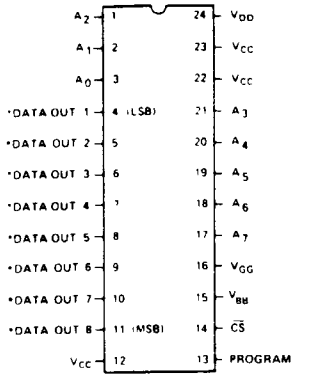
The 1602A and 1702A use identical chips. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The 1602A is packaged in a 24 pin dual in-line package with a metal lid and is not erasable.

The circuitry of the 1602A/1702A is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is ideal for large volume production runs of systems initially using the 1602A or 1702A.

The 1602A/1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

PIN CONFIGURATION



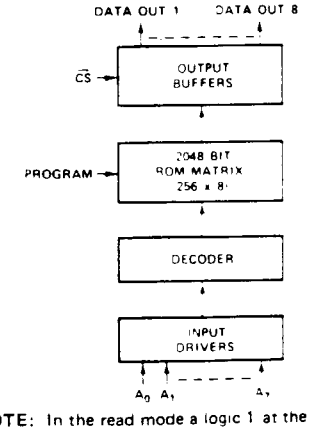
*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

See page 3-8 for operational connection.

PIN NAMES

A_0–A_7	Address Inputs
$\overline{CS}$	Chip Select Input
D_{OUT1}–D_{OUT8}	Data Outputs

BLOCK DIAGRAM



NOTE: In the read mode a logic 1 at the address inputs and data outputs is a high and logic 0 is a low.

U.S. Patent No. 3660819

*Intel's liability shall be limited to replacing any unit which fails to program as desired.

PIN CONNECTIONS

The external lead connections to the 1602A/1702A differ, depending on whether the device is being programmed or used in read mode. (See following table.) In the programming mode, the data inputs 1-8 are pins 4-11 respectively.

MODE \ PIN	12 (V_{CC})	13 (Program)	14 ($\overline{CS}$)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Absolute Maximum Ratings*

Ambient Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Soldering Temperature of Leads (10 sec) . . . . . +300°C
Power Dissipation . . . . . 2 Watts
Read Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . +0.5V to −20V
Program Operation: Input Voltages and Supply Voltages with respect to V_{CC} . . . . . −48V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC} = +5V±5%, V_{DD} = -9V±5%, V_{GG}[1] = -9V±5%, unless otherwise noted. Typical values are at nominal voltages and T_A = 25°C.

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	µA	V_{IN} = 0.0V
I_{LO}	Output Leakage Current			1	µA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC} −2
I_{DDO}	Power Supply Current		5	10	mA	V_{GG}=V_{CC}, $\overline{CS}$=V_{CC}−2, I_{OL} = 0.0mA, T_A = 25°C — Note 1
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 25°C
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$=0.0, I_{OL} =0.0mA, T_A = 25°C
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS}$=V_{CC} −2, I_{OL} =0.0mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
I_{GG}	Gate Supply Current			1	µA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC} −6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC} −2		V_{CC} +0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		−.7	0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100 µA

NOTE 1: POWER-DOWN OPTION: V_{GG} may be clocked to reduce power dissipation. The average I_{DD} will vary between I_{DDO} and I_{DD1} depending on the V_{GG} duty cycle (see typical characteristics). For this option please specify 1702AL or 1602AL.